Power Optimization using 4-bit Ripple Carry Adder and 4-bit Carry Look Ahead Adder at various Technology Nodes, Supply Voltages and Multi-Threshold Voltages

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**Abstract – In electronics, an adder that is also known as summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in the other parts of the processors, where they are used to calculate addresses, table indices, and similar operations. Here, we have constructed a half adder and then with the help of the half adder we have built a 1-bit full adder that will have 3 inputs and 2 outputs (Sum and Carry. Using 4 1-bit full adders, we have built a 4-bit RCA (Ripple Carry Adder) and also we have built CLA (Carry Look Ahead Adder) to solve the truth table (Fig). Further we have written the HSPICE and simulated the logic design for different CMOS technology nodes. By simulating the code we have measured the power dissipation and the delay. We also use Cosmosscope to check the given input and output signal.**

1. Introduction

Low Power Design is one of the most important aspects and also most required topic for most adversely developing technology. Until recent times the power dissipation of electronic components was considered only as a small fraction. But, now low power is very much required to improve the battery back up and also for its high performance as use of portable devices have been drastically increased. Low power is not only important for battery, it is also important for many portable devices that run on the battery, to name few its laptop, tablet, Computer, cell phone, I-pod, I-pad etc. In these devices there will be more power dissipation since high supply voltage will be given to the low power components in the device.

According to Moore’s Law the use of integrated circuit elements will increase rapidly every decade, may be in terms of millions and billions. This may increase the speed or may also increase the power usage. Hence, we must develop designs such that it will make use less power and also increases the operation of the IC elements. This could be done by the help of Low Power Design Technology.

In Low Power IC Design, we design electronic elements that use less electric power and also occupy less total area. Low Power IC Design is a subject that deals with the problems such as Power Dissipation, Power Consumption and also the operational speed. Nowadays it is very important to design a circuit with less power consumption and also with more operational speed. Therefore, we should design a circuit that consumes less power as well as has less dissipation. And to achieve this we should build a small circuit with low power consumption and low power dissipation and also use limited elements that consume more power.

Through this project we would like to show that we could decrease the power dissipation by decreasing the supply voltage, by increasing the threshold voltage of PMOS and NMOS and also by checking what happens when we decrease the length of the transistors we use. Therefore, we are going to built RCA and CLA and simulate them by reducing the supply voltage and also by using different technology and also giving various threshold voltages. We use NAND, AND and OR gates to build the RCA and CLA circuits. The main objective or goal of our project is to reduce the power dissipation and also to increase the speed operation. For this we use theoretical explanation where total Power dissipated in a CMOS circuit is sum total of dynamic power, short circuit power and static or leakage power.

1. Methodology and Tools

We know that NAND gate is a universal gate and hence we can use this to design any type of digital circuits. In this project we have built a RCA and CLA circuits and we have checked its outputs to find power dissipation and operational speed in different conditions.

The different conditions that we have applied are :

1. Different Technology

2) Supply voltage

3) Multi-threshold voltage.

First, we designed a half adder that is shown in Fig.1 below. Half adder will have 2 single binary inputs and 2 outputs Sum (S) and Carry (C). The carry signal represents an overflow into the next digit of multi-digit addition. We have used this to build to design 1 bit Full Adder. Then we have expanded this to build RCA and also CLA. As both RCA and CLA has different designs we use full adders in different numbers and also for CLA we use AND-OR gates as well. After building these circuits we just check the output for different voltage supply and also for different threshold voltages.

To be more specific we have decreased supply voltage by 0.1 for all technology and checked the dynamic power dissipation, static power dissipation and delay for each case. By decreasing the supply voltage we found that the dynamic power dissipation and static power dissipation will be decreased. But, the delay has increased decreasing the operational speed.

We have increased the threshold voltage by 20% and applied to all the cases and we found that when we increase the threshold voltage the dynamic power dissipation and static power dissipation will be decreased. But, the delay has increased decreasing the operational speed.

We have approximately tested more than 50 cases.

The technology nodes we have selected is 65nm, 45nm, 32nm PTM BSIM4 models (published on Feb. 22, 2006). 32nm and 22nm nodes (PTM metal gate/high-k CMOS V2.0 models, Release date :October 29, 2007). All 5 models were taken from the below website <http://www.eas.asu.edu/~ptm>. The simulation conditions are as follow:

.include (technology file).txt

.temp 100

.tran 1ps 60ns

The width of the PMOS transistor is taken as 2.5 times of the width of the NMOS transistors. The leakage current is calculated for the entire simulation duration. In static case the input selections are as follows: A3 to A0 = 0000 to 1111.

We should know about the RCA and CLA design as we have used these to check the difference in the power dissipation and speed between them.

Half adder is given below

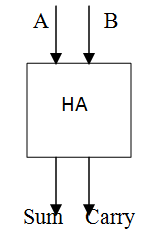


Figure: 1(a) –Half Adder

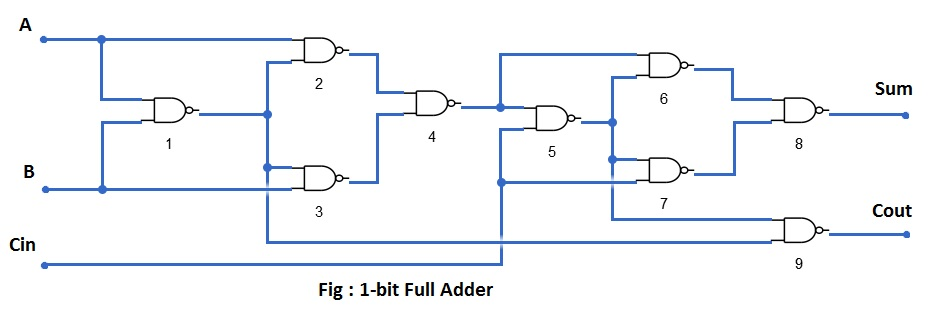
We combine two half adder to build a full adder.

For a full adder sum and carry are given by:

**Full Adder:**

Sum = a ⊕ b ⊕ c

Cout = a • b + c • (a ⊕ b )



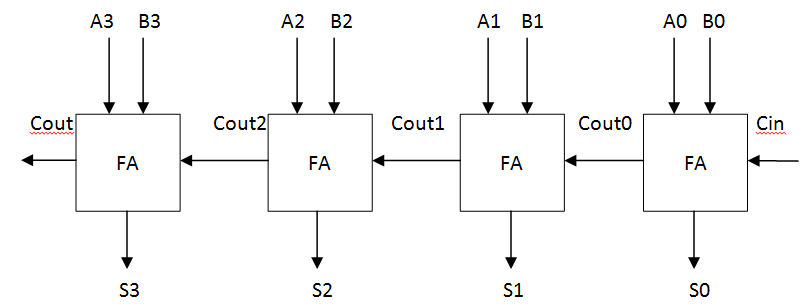


Figure 2(a)- 4-bit Full Adder

Above is the 1 bit full adder with A, B and Cin as the three inputs and sum and carry as the output. We have used four such full adders and built a 4-bit Full Adder. We have used this 4-bit full adder along with 2 AND gates and 2 OR gates for the CLA where the AND and OR gates are used to get carry output.

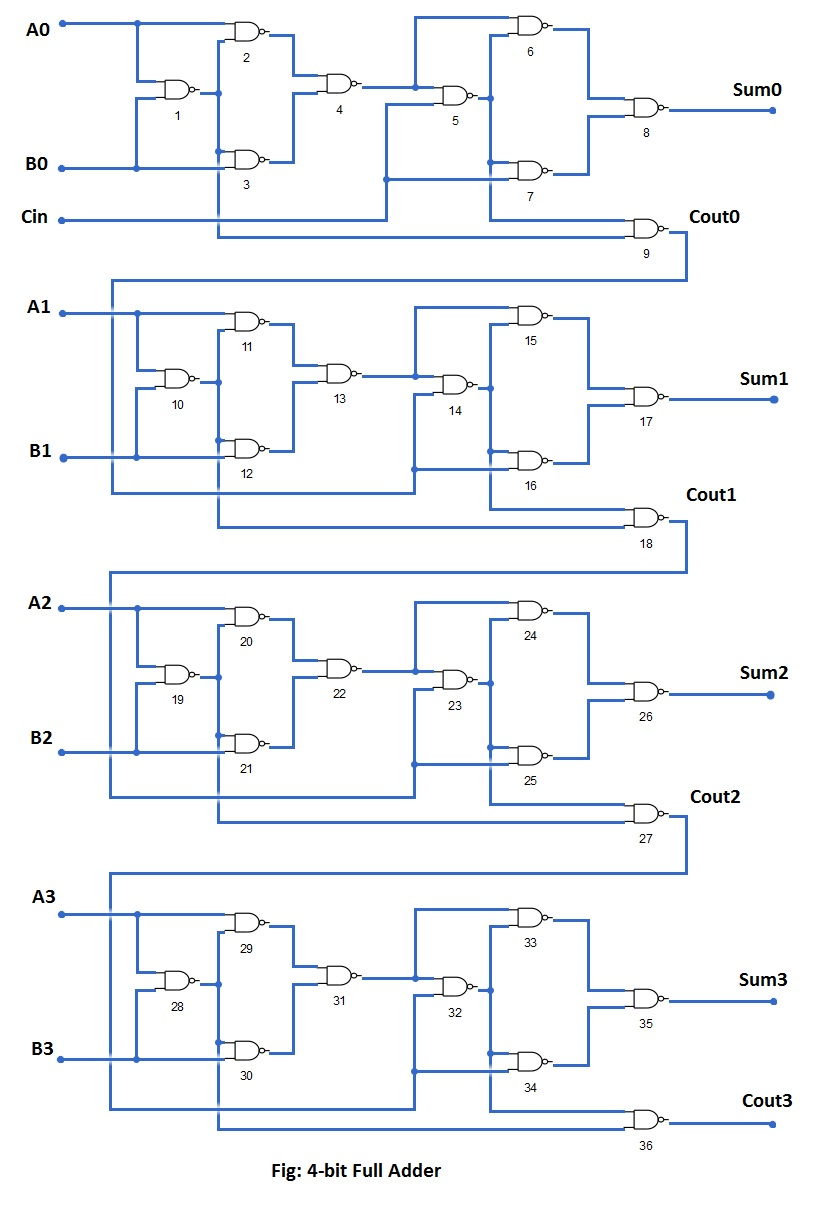


Figure 2(b)

**Carry Look Ahead Adder:**

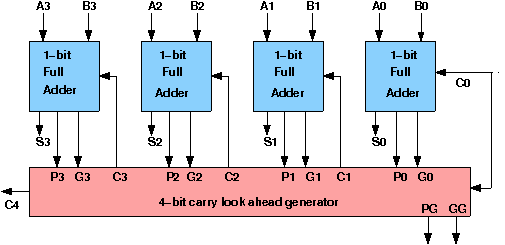


Figure 3(a)- 4-bit Carry Look Ahead Adder.

Sum = a ⊕ b ⊕ c

**![](data:application/pdf;base64,)**

Cout = Gi + Pi\* Ci

Pi = A+B

Gi = A.B

Truth table below is same to both RCA and CLA ( ABC from 000 to 111)

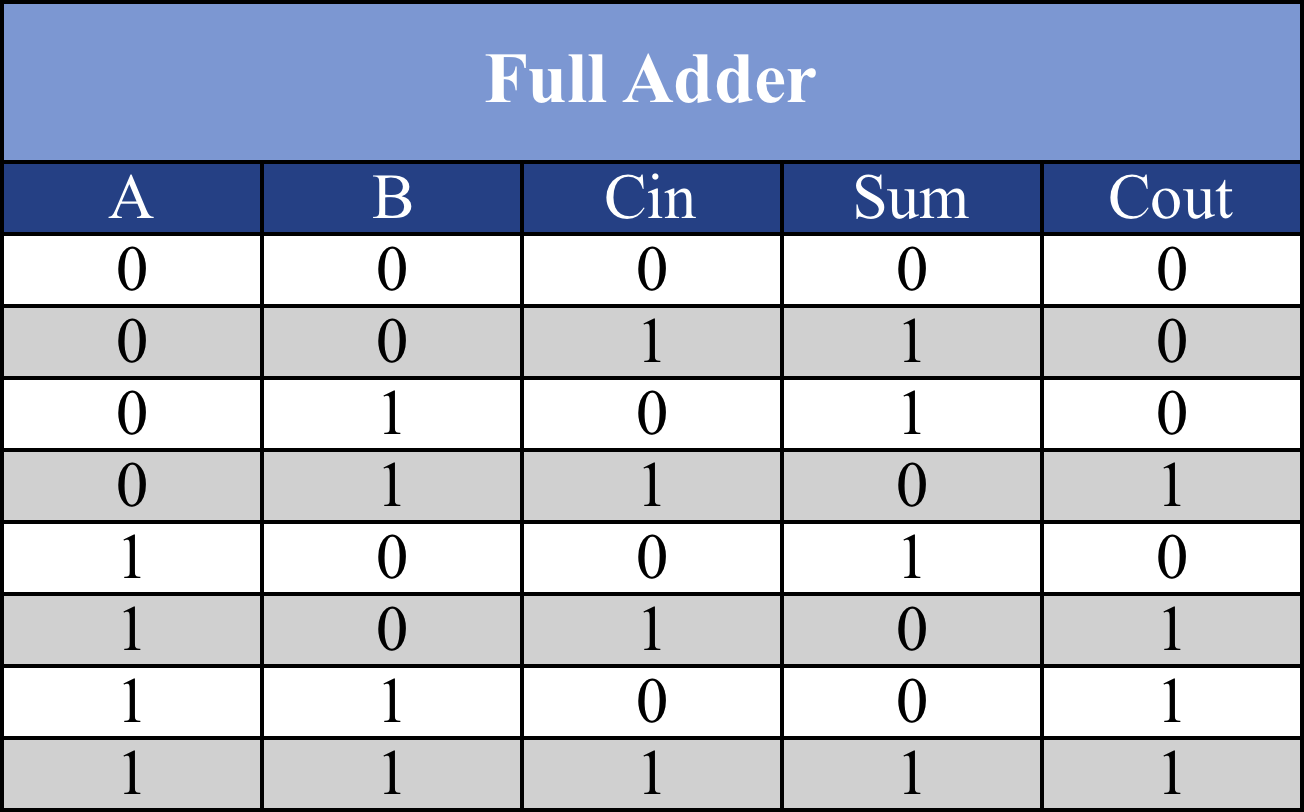


Table 1- Full Adder (both RCA and CLA)

After building these circuits we just wrote the HSPICE code for both RCA and CLA to find the dynamic power dissipation, time delay and also leakage current from which we find the static power dissipation.

Figure 3(b)

iii) Observations based on the Output of the HSPICE Code:

Basically we gave different voltages for different technologies and then we reduced those voltages by 0.1 and found the difference in the two outputs we got. We also executed the codes for increased multi-threshold voltages.

**For RCA**

Case 1: Baseline and Reduced supply voltages

i) Dynamic Power

Here we can observe that there is a reduction in the dynamic power dissipation thereby proving the theoretical explanation that is, when we decrease voltage the power dissipation will reduce.



Figure 4(a)

Figure 4(b)

ii) Static Power.



Figure 5(a)

Figure 5(b)

From the above table and the graph we can observe that there is a reduction in the static power due to reduction in the supply voltage

iii) Time Delay:

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Figure 6 (a)

Figure 6 (b)

Here we can observe that there is an increase in the time delay due to reduction in the supply voltage. This will decrease the operational speed and thereby decreasing the performance of the circuit.

Case 2: Baseline with Multi-Threshold Voltage

i) Dynamic Power



Figure 7(a)



Figure 7(b)

When the threshold voltage is increased then the dynamic voltage is reduced.

ii) Static Power



Figure 8(a)

Figure 8(b)

When the threshold voltage is reduced then the static voltage will reduce.

iii) Time Delay

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Figure 9(a)

Figure 9(b)

Due to increase in the Vth the time delay will increase leading to decrease in the performance.

**For CLA**

Case1: Baseline and Reduced Supply Voltage

1. Dynamic Power

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Figure 10(a)

Here we can observe that there is a reduction in the dynamic power dissipation thereby proving the theoretical explanation that is, when we decrease voltage the power dissipation will reduce.

Figure 10(b)

1. Static Power

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Figure 11(a)

Figure 11(b)

From the above table and the graph we can observe that there is a reduction in the static power due to reduction in the supply voltage

1. Time Delay

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Figure 12(a)

Figure 12(b)

Here we can observe that there is an increase in the time delay due to reduction in the supply voltage. This will decrease the operational speed and thereby decreasing the performance of the circuit.

Case 2: Baseline and Increased Vth:

1. Dynamic Power

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Figure 13(a)

Figure 13(b)

When the threshold voltage is increased then the dynamic voltage is reduced.

1. Static Voltage:

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Figure 14(a)

Figure 14(b)

When the threshold voltage is reduced then the static voltage will reduce.

1. Time Delay

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Figure 15(a)

Figure 15(b)

Due to increase in the Vth the time delay will increase leading to decrease in the performance.

From all the above observations we found that when the supply voltage is reduced then there will be reduction in the power dissipation but at the same time there will be increase in delay thereby affecting the performance.

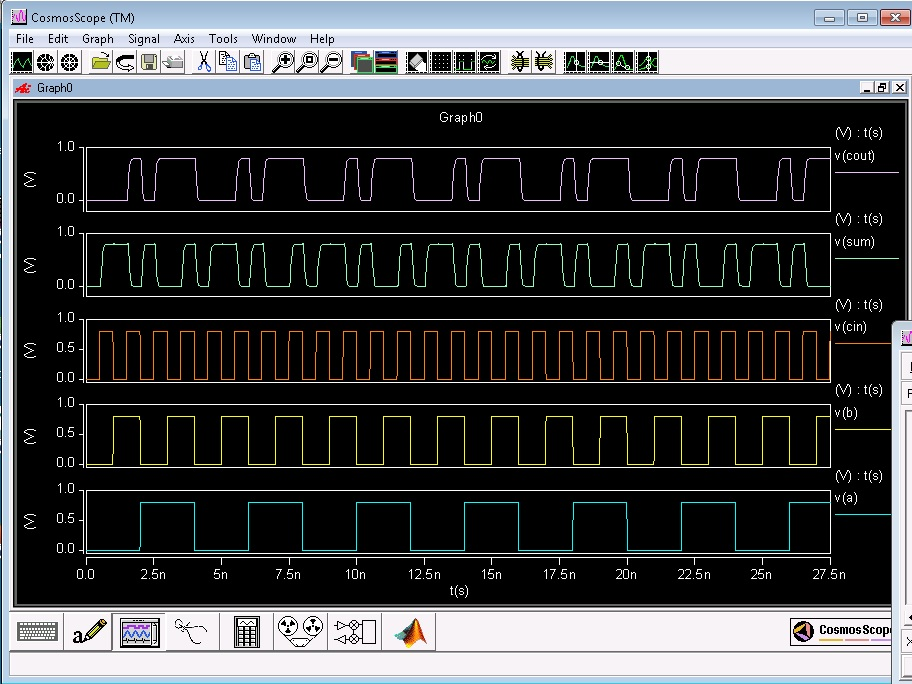
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Figure 16- Full adder i/p and o/p

1. Results:

Taking consideration of all the above observations we can come to a conclusion that we can reduce the power dissipation by reducing the supply voltage and also increasing the threshold voltage. But both have a drawback where in decreasing the supply voltage and increasing the threshold voltage will affect the performance. Therefore in future we have to work on the things where we can maintain both decrease in the power dissipation and the performance equally. That is when we decrease or increase the supply voltage or threshold voltage there should be less affect for the performance and more affect on decrease in the power loss.

Therefore, if we decrease the threshold voltage we will be increasing the power dissipation but will be decreasing the delay allowing high performance. But in this case again we have to take the power loss into consideration.

1. Future Work

Overall we have observed and we succeeded in reducing the power dissipation in both RCA and CLA. But we prefer CLA instead of RCA for the higher performance as CLA will not wait for the Cin to generate Sum. Hence we can reduce the threshold voltage for CLA and make it still faster. But we will have to deal with the power dissipation in this case. Hence in future we should work on reducing the threshold voltage for CLA circuit and to improve its performance. Therefore, we use CLA more when speed of the operation is dominant over the power loss.

In general we should work on the fact that when we use a technique to reduce the power dissipation it should also show more importance on reducing the delay so that the performance will also not affected.

1. Conclusion:

Overall we have observed and we succeeded in reducing the power dissipation in both RCA and CLA. In this project we have succeeded in achieving power optimization using 2 techniques. We have implemented the circuits and simulated them to obtain the expected results. We have developed more ideas and ways to further optimize the power dissipation and performance we would want to test in future work.

Reference:

[1] Design and simulation of low power reconfigurable RCA and CLA by using DMFA and HBFA- M. Manikandan and Shiju C

[2] Low power design essential by Jan Rabaey

[3] <https://en.wikipedia.org/wiki/Adder_(electronics>)

[4] <http://www.utdallas.edu/~poras/courses/ee3320/xilinx/upenn/lab4-CarryLookAheadAdder.htm>

[5] Lecture given in the class on Low Power IC Design by Professor Pradeep Nair